

In re Patent Application of:

BHARDWA ET AL

Serial No. **09/977,065**

Filed: **OCTOBER 12, 2001**

Remarks

Claims 1-39, 41, 44, and 45 are pending in this application.

Claim 41 is allowed and claims 8, 12, 21, 25, 34, and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if re-written in independent form, including all of the limitations of the base claim and any intervening claims.

Claims 8, 12, 21, 25, 34, and 38 have been rewritten in independent form and are now believed to be allowable.

Claims 1-4, 6-7, 9-11, 13-17, 19-20, 22-24, 26-30, 32-33, 35-37, 39 and 44-45 have been rejected under 35 U.S.C. § 102 (b) as being anticipated by Bhagavatula US 5,125,946 hereafter referred to as '946.

The office action states that regarding claims 1, 14, and 27, Figure 7 of '946 teaches a planar lightwave circuit, and therefore methods for forming and balancing stress in the same, comprising at least one optical waveguide core (5); at least one feature (6,4) proximate the core having at least one stress engineered property to balance stress and therefore minimize birefringence affecting the core; and a protective passivation layer (9) formed over the core and the feature the passivation layer formed to be substantially non-interfering with the balanced stress affecting the core provided by this feature.

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It is the applicant's view that claims 1, 14 and 27 each define a patentable invention over the teachings of the '946 patent.

Claim 1 of the instant invention reads as follows:

1. A planar lightwave circuit, comprising:
at least one optical waveguide core;
at least one feature proximate the core having at least one stress-engineered property to balance stress and therefore minimize birefringence affecting the core; and
a protective passivation layer formed over the core and the feature, the passivation layer formed to be substantially non-interfering with the balanced stress affecting the core provided by the feature.

The '946 patent in Fig. 7 shows the following



Fig. 7

The applicant respectfully disagrees with the statement that '946 teaches a planar lightwave circuit, and therefore methods for forming and balancing stress in the same, comprising at least one optical waveguide core (5); at least one feature (6,4) proximate the core having at least one

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stress engineered property to balance stress and therefore minimize birefringence affecting the core.

Layer 4 is referred to by Bhagavatula in '946 as a barrier layer selected to provide a suitable refractive index difference between itself and the core to channel the majority of light incident on the waveguide through the core layer. Essentially this barrier layer is a cladding. The following excerpts are taken from the '946 patent:

"The layers of material so applied preferably consist of a barrier layer 4, core layer 5, and clad layer 6 as shown in FIG. 2."

"Whether barrier layer 4 is used depends on the refractive index and loss characteristics of the substrate 1. If the refractive index differential between substrate 1 and core layer 5 is too small, the material of the barrier layer 4 is selected such that the refractive index differential between the barrier layer and the core layer is sufficient to channel the majority of the light incident on the resulting planar optical waveguide through core layer 5. The refractive index of clad layer 6 is also selected to enable efficient waveguide propagation through core layer 5."

"A barrier layer 4, as shown in FIGS. 2-7, is not required because the substrate is fused silica and has the necessary refractive index in relation to the refractive index of the core layer 5. A cross-section of the cane used in this example, without a barrier layer, is shown in FIG. 8. References to FIGS. 2-7 in describing the lithographic process

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used in this example will be made for convenience only, as FIGS. 2-7 show a barrier layer which is not present in this example. A core layer 5 (FIG. 8) approximately 100 .mu.m thick, consisting of SiO.sub.2 and 8% by weight GeO.sub.2, with a refractive index of approximately 1.464, is applied to the substrate. Thereafter a clad layer 6 of pure silica soot approximately 100 .mu.m thick is applied over the core layer."

There is no hint or suggestion that the barrier layer 4 or the cladding layer 6 have a stress-engineered property to balance stress and minimize birefringence in the core.

The only teaching within the specification of the cited reference that mentions stress is the following passage:

"Another alternative is to etch precise dimensional slots 14 in substrate 1 which correspond to the preselected optical circuitry shown in FIG. 11(a). Thereafter at least one shaped (e.g., circular, square, elliptical or D-shaped) optical fiber preform or large core optical fiber 15 (hereinafter optical fiber preform 15) with core regions 16, 16' having the desired refractive index profile (e.g., step or graded) is placed in at least one of slots 14. The optical fiber preform may alternatively consist of a core only. In addition, stress inducing materials or members may be included to provide stress birefringence."

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This is most certainly "not" disclosure of a stress-engineered property to balance stress and minimize birefringence in the core

There is no teaching in the '946 reference of a passivation layer and no mention of a layer that could function as passivation layer. The examiner has attributed this functionality to layer 9, which is said to be an overcladding silica layer. One skilled in the art would not make this association since an overcladding layer is not a passivation layer covering an overcladding. An overcladding is merely an upper cladding, and the applicant has disclosed and claimed a passivation in addition to an overcladding, wherein the passivation layer is defined in a novel manner in relation to the overcladding and the stress engineered feature.

The examiner suggests that since '946 teaches that a substrate is selected to match thermal properties of the waveguide conductors and films, that a passivation layer (9) formed over the core and the feature is to be non-interfering.

However, there is simply no such teaching or suggestion of this. As was stated earlier, the '946 reference makes no mention of a passivation layer, and clearly makes no mention of a passivation layer that is matched so as to not interference with a stress engineered property.

This is not suggested or inherent from the statement that the substrate should be selected to match the thermal and mechanical properties of the materials used as waveguides and films. It is common knowledge that when a substrate is to be

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selected, that it should be closely matched in CTE to cladding layers if it can be, and since the substrate is merely a support upon which to build subsequent layers, this is typically done. Notwithstanding, this is not a teaching of providing a passivation layer on a waveguide structure with a stress engineered property, wherein the passivation layer is also engineered to be CTE matched so as to avoid unwanted birefringence. Heretofore, no one has proposed considering matching the coefficient of thermal expansion of a thin nitride layer so that it would not induce unwanted stress when applied to a special feature designed to reduce stress. Since the applicant has a structure where not all of the layers can have a matched CTE, the layers are carefully constructed with a special feature near the core to lessen stress and wherein a particular thickness and doping of a passivation layer does not interfere with this balanced PLC it protects. It is this combination that is novel and inventive.

Kawachi requires laser trimming afterwards to make his structure useful. He did not suggest the applicant's special passivating layer in combination with a special stress reducing feature alleviating stress. In fact Kawachi taught away from such a notion.

Kawachi taught irradiation of his finished structure to attempt to balance stresses so as to trim the "unbalanced" device he manufactures.

With regard to claims 2, 15, and 28, '946 is said to teach a planar lightwave circuit and methods wherein the at least one feature comprises an overcladding layer (6) formed

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over the core (5) and doped to balance stress affecting the core.

Claim 2 of the instant application defines:

2. The planar lightwave circuit of claim 1, wherein the at least one feature comprises an overcladding layer formed over the core, and doped to balance stress affecting the core.

Claim 2 when read with the limitations of claim 1 reads as follows:

2. A planar lightwave circuit, comprising: at least one optical waveguide core;
at least one feature proximate the core having at least one stress-engineered property to balance stress and therefore minimize birefringence affecting the core; and,
a protective passivation layer formed over the core and the feature, the passivation layer formed to be substantially non-interfering with the balanced stress affecting the core provided by the feature, wherein the at least one feature comprises an overcladding layer formed over the core, and doped to balance stress affecting the core.

In this claim, a waveguide core, an overcladding having a feature near the core with a stress engineered property and doped to balance stress AND a passivation layer wherein the passivation layer is substantially non-interfering with the balanced stress affecting the core provided by the feature is defined.

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The so-called passivation layer recited by the examiner as (9) in the '946 reference is defined in the specification to be an overcladding layer;

The examiner has stated in the rejection of claim 2 that the overcladding layer (6) is doped to balance stress affecting the core. However the applicant has not found such disclosure anywhere in the specification. The examiner has recited Col 3 lines 29-31 and applied this teaching to specific instances where such teaching does not occur. For example, Col 3 lines 29-31 states:

The material of the substrate is selected to match the thermal and mechanical properties of the materials used as waveguide conductors and films.

This is basic knowledge in the industry. Selecting a substrate that is compatible with the materials being deposited upon it is well known.

Notwithstanding, this does not teach or suggest providing a stress engineered feature to balance birefringence (in fact it is in contrast with it) and providing a passivation layer that is CTE matched so that it does not interfere with the stress engineered feature. In summary, there is no such teaching in the cited '946 reference of providing the stress engineered feature by way of an overcladding layer (6) and doped to balance stress affecting the core.

The limitations of claim 2 have been incorporated into claim 1 and amended claim 2 now defines:

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The planar lightwave circuit of claim 1, ~~wherein the at least one feature comprises an overladding layer formed over the core, and doped to balance stress affecting the core~~ wherein the overladding and the passivation layer have a matched CTE and together provide the balanced stress to counter stress within the core, thereby minimizing the overall birefringence.

Neither of the two cited references suggest providing an overladding and passivation which together are CTE matched and which together provide a balanced stress minimizing the overall birefringence.

Claims 4, 17, and 30 have been rejected in view of the '946 reference which the examiner asserts teaches a planar lightwave circuit and methods wherein a protective passivation layer (9) is formed to have a coefficient of thermal expansion approximately matched to that of the overladding such that it is substantially non-interfering.. Col 3 lines 29-31 and 52-53.

The applicant respectfully disagrees with this summary. Layer (9) is not a passivation layer; it is an overladding layer. Furthermore, there is no mention of this layer being matched in CTE to that of the overladding; it is the overladding; and there is no mention of this overladding being matched to that of an overladding as to be in any way so as to be unaffected balanced stress affecting the core provided by the overladding, since it is the overladding. Furthermore, the applicant must once again point out that providing CTE matched layers is not novel and as the examiner

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correctly notes, Bhagavatula teaches matching the index of the substrate with other layers thereon; however there is an important, significant difference. The applicant provides a stress balancing feature, within these layers so as to finely tune the device; CTE matching is the substrate and overcladding is only a first and obvious step; providing doping sufficient to ALSO induce a stress balance and further provide a passivation layer that will not negate this stress balance is a "true" advance in the art. Kawachi who had access to the teachings of Bhagavatula did not recognize this, and had to laser tune is manufactured devices.

Claims 5, 18, 31 are rejected as being unpatentable over Bhagavatula in view of Kawachi, United States Patent 4,900,112.

Claim 5 with all of the limitations of the claims from which it depends defines:

A planar lightwave circuit comprising:

a substrate;

at least one optical waveguide core;

an undercladding formed over the substrate and under the core;

at least one feature proximate the core having at least one stress-engineered property to balance stress and therefore minimize birefringence affecting the core, wherein the one feature comprises an overcladding layer formed over the core, and doped to balance stress affecting the core wherein the overcladding is doped to have a

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coefficient of thermal expansion approximately matched to that of the substrate to thereby symmetrically distribute stress in the undercladding between the overcladding and the substrate, and therefore away from the core ; and

a protective passivation layer comprising silicon nitride formed over the core and the feature, the passivation layer have a coefficient of thermal expansion approximately matched to that of the overcladding such that it is substantially non-interfering with the balanced stress affecting the core provided by the overcladding.

Claim 5, as re-written in claim 1 in independent form to include all of the limitations of claims from which it depends, defines a novel and inventive structure not suggested or disclosed by either Bhagavatula or Kawachi, alone or in combination.

The applicant has defined a waveguide structure having a stress engineered feature and doped to have a CTE matched to that of the substrate to thereby symmetrically distribute stress in the undercladding between the overcladding and the substrate, and therefore away from the core.

In addition to this, the claim is restricted to having a protective passivation layer comprising silicon nitride formed over the core and the feature, the nitride passivation layer having a coefficient of thermal expansion approximately matched to that of the overcladding such that it is substantially non-interfering with the balanced stress affecting the core provided by the overcladding.

Neither Kawachi or Bhagavatula suggested a feature providing balanced stress, and a passivation layer that is designed to be non-interfering with the balanced stress.

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Kawachi makes no mention of matching the CTE of the silicon nitride passivation layer with that of the overcladding. In fact, Kawachi goes to great lengths to overcome stress however does so in a completely different brute force manner.

Instead of designing his structure so that it is stable and such that the passivation layer induces no stress upon the combination of layers beneath it that are precisely stress balanced, he is forced to use laser trimming after applying the passivation layer to achieve some reduction in stress. The applicant on the other hand teaches and claims a structure that takes is stress engineered and doped to have a CTE matched to that of the substrate to thereby symmetrically distribute stress in the undercladding between the overcladding and the substrate, and therefore away from the core. Furthermore, the applicant discovered the deleterious effect of simply applying the silicon nitride passivation layer without considering induced stress. Fabricating in such a manner produces inferior devices and the applicant has provided a solution to this problem by way of this invention. The applicant after providing the stress inducing feature to balance stresses carefully provides the silicon nitride layer with the a CTE so as to not unbalance the induced stress provided by the claimed feature.

In summary, neither of the cited references provides this solution nor achieves its inherent advantage. No laser trimming is required, as the applicant does not require correction after his nitride layer is deposited.

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Heretofore, it was unknown to consider the effect of this thin passivation layer; however the advantage of ensuring that it does not affect the stress in the underlying finely tuned device is significant. It should also be understood that specific doping levels must be used in order to achieve this advantage.

Claim 1 has been amended and limited to include all of the limitations of claims 2 through 5.

Claim 1 now defines:

A planar lightwave circuit comprising:

a substrate;

at least one optical waveguide core;

an undercladding formed over the substrate and under the core;

at least one feature proximate the core having at least one stress-engineered property to balance stress and therefore minimize birefringence affecting the core, wherein the one feature comprises an overcladding layer formed over the core, and doped to balance stress affecting the core wherein the overcladding is doped to have a coefficient of thermal expansion approximately matched to that of the substrate to thereby symmetrically distribute stress in the undercladding between the overcladding and the substrate, and therefore away from the core (having a different CTE) ; and

a protective passivation layer comprising silicon nitride formed over the core and the feature, the passivation layer have a coefficient of thermal expansion approximately matched

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to that of the overlcladding such that it is substantially non-interfering with the balanced stress affecting the core provided by the overlcladding.

Neither Kawachi or Bhagavatula disclose the novel and inventive combination of providing a waveguide core with an undercladding and an overlcladding wherein one feature is near the core having a stress engineered property to balance stress and minimize birefringence affecting the core wherein the feature includes the overlcladding layer doped to balance stress wherein the overlcladding CTE is matched to the cladding to symmetrically distribute stress in the undercladding between the overlcladding and the substrate and away from the core AND including a passivation layer of silicon nitride having a CTE matched to the overlcladding such that is is substantially non-interfering with the balanced stress affecting the core provided by the overlcladding.

The '946 patent teaches nothing more than selecting a substrate material to be thermally matched with materials used as waveguide conductors and films. The applicant on the other hand has a much more complex structure, wherein certain layers cannot be CTE matched and require features to minimize stress other than CTE matching; the applicant further teaches and claims CTE matched layers which provide stress minimization and, a passivating layer that is specifically tailored to be matched to a layer upon which it is deposited. The cited Kawachi reference teaches the use of a silicon nitride layer as a passivation layer, but does not teach a specific doping and thickness of that layer that will allow it to be deposited such that it does not disturb the underlying structure.

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In the background of the invention the applicant states that:

"Waveguides are typically fabricated by forming (e.g., etching) waveguide core patterns over a substrate and undercladding. A doped glass overcladding (e.g., borophosphate silicate glass or BPSG) is then formed over the cores, to complete the waveguide formation. Because the materials used for these layers are different, with differing properties (e.g., differing coefficients of thermal expansion (CTEs)), intra- and inter-layer stresses exist and will result in high levels of waveguide PDL."

The applicant has provided and claimed a particular combination of layers that overcome this. The layers are not all CTE matched, as they cannot be. Some are matched and some require special stress features. It is this special unique combination that provides a superior device that is practicable.

The specification of the instant invention clearly states: "Regardless of the particular selection of stress balancing features, the passivation layer is designed to be non-interfering with their stress balancing properties, while providing all of the benefits of passivation, including its barrier to vapor, chemicals, etc. This barrier protection is becoming increasingly important as optical components are subjected to more adverse environments, and their related reliability standards and testing."

The provision of this special passivation layer is novel. It is not the same layer that Kawachi discloses. It has

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a thickness and doping to yield a desired result, not taught by Kawachi. No one has before contemplated matching a passivation layer in this manner. It is the applicant's belief that heretofore, no one has realized the impact a thin passivation layer could have on the stress of the device.

The specification teaches: "This overlcladding layer 106 may be tailored for stress engineering, as follows: The primary stress in the system results from the CTE mismatch between the silicon layer 100 and the thermal oxide layer 102. For example, the CTE of layer 100 may be on the order of 3.5 parts per million (ppm), and that of layer 102: 0.7 ppm. The silicon layer 100 therefore contracts at about five times the rate of the thermal oxide layer 102. Though this stress is highest at this layer interface, the stress field extends to the upper surface of layer 102, to its interface with the cores (which themselves have a CTE of approximately 2.05 ppm)."

The specification further teaches a specific enabling example of silicon nitride that was not contemplated by either of the cited references: "For example, a silicon nitride film can be used (e.g., Si₃N₄) with a thickness of .55μm optimized for stress of approximately -40+/-5Mpa. A plasma etched chemical vapor deposition (PECVD) process is used, with a deposition rate of approximately 1800 Å/min, 445 watts power @ 13.5 MHz, 555 watts @ 2.27 kHz, Ts=400 C, and pressure=3.3 torr. Exemplary deposition flows are: N₂=1600 sccm, SiH₄=500 sccm, NH₃=4000 sccm, with a resultant film refractive index of approximately 2.0350, and CTE of 3.4 ppm, i.e., approximately matched to that of BPSG layer 106. Passivation layer 108

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therefore does not add any stress to the previously stress-engineered system over which it is deposited."

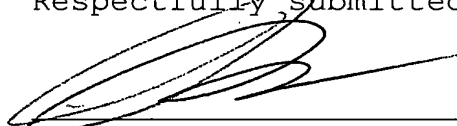
In view of the foregoing, it is respectfully submitted that all of the claims remaining in the application are in condition for allowance.

Early and favorable consideration would be appreciated.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 50-1465 and please credit any excess fees to such deposit account.

Respectfully submitted,



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A handwritten signature in cursive script, appearing to read "J. Murphy", written over a horizontal line.